Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A data processing apparatus, for receiving a communication signal that comprises a message containing a sync break interval with a unique bit pattern, the message containing a sync field interval identified by the sync break interval, a timing property of the sync field interval specifying a length of bit periods of the message, the apparatus comprising:

an input port for receiving the communication signal;

a reception circuit for sampling and processing bits from the message;

a clock source circuit for supplying a sampling clock signal to the reception circuit to define time points for said sampling, the clock source circuit being arranged to adapt a frequency of the sampling clock signal to the timing property of the sync field interval, the clock source circuit being arranged to search for potential sync break intervals that match the unique bit pattern for a range of bit period values, the clock source circuit verifying for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval, wherein the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met.

2. (canceled)

3. (original) A data processing apparatus according to claim 1, wherein said unique pattern contains a repetition of a same bit value for more than a maximum number of bit periods during which the same bit value is permitted to be repeated during a remainder of the message.

4. (canceled).

5. (original) A data processing apparatus according to claim 1, wherein the clock source circuit operates in parallel with the reception circuit, proceeding with said searching while said reception circuit is sampling bits from the communication signal.

6. (original) A data processing apparatus according to claim 1, wherein the clock source circuit comprises a local clock circuit for generating a local clock signal, counter means for counting respective first numbers of periods of said local clock signal that occur in the potential sync break intervals and respective second numbers of periods of the local clock signal that characterize the timing property of the sync field intervals identified by the potential sync break intervals and a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range.

7. (currently amended) A method of sampling data from a communication signal in a data processing apparatus, wherein the communication signal ~~that~~ comprises a message containing a sync break interval with a unique bit pattern, the message containing a sync field interval identified by the sync break interval, a timing property of the sync field interval specifying a length of bit periods of the message, the method comprising

supplying a sampling clock signal to define time points for sampling bits from the message, said supplying comprising:

searching for potential sync break intervals that match the unique bit pattern for a range of bit period values,

verifying for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period,

supplying the sampling clock signal at a frequency adapted to the timing property of the sync field interval on the condition that the sync break interval matches the unique pattern for the specified bit period, wherein the supply of the sampling clock signal is suppressed after an end of a preceding message until said condition is met.

8. (new) A data processing apparatus configured to receive a communication signal that comprises a message that contains a sync break interval with a unique bit pattern, the message containing a sync field interval identified by the sync break interval, a timing property of the sync field interval specifying a length of bit periods of the message, wherein the apparatus comprises:

an input port to receive the communication signal;

a reception circuit to sample and to process bits from the message;

a clock source circuit to supply a sampling clock signal to the reception circuit to define time points for the sampling, wherein the clock source circuit, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval, is further configured to adapt a frequency of the sampling clock signal to the timing property of the sync field interval, to search for potential sync break intervals that match the unique bit pattern for a range of bit period values, to verify for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, to verify whether one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval, and to suppress the supply of the sampling clock signal after an end of a preceding message until said condition is met.

9. (new) A data processing apparatus according to claim 8, wherein said unique pattern contains a repetition of a same bit value for more than a maximum number of bit periods during which the same bit value is permitted to be repeated during a remainder of the message.

10. (new) A data processing apparatus according to claim 8, wherein the clock source circuit operates in parallel with the reception circuit, proceeding with said searching while said reception circuit is sampling bits from the communication signal.

11. (new) A data processing apparatus according to claim 8, wherein the clock source circuit comprises a local clock circuit for generating a local clock signal, counter means for counting respective first numbers of periods of said local clock signal that occur in the potential sync break intervals and respective second numbers of periods of the local clock signal that characterize the timing property of the sync field intervals identified by the potential sync break intervals and a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range.

12. (new) The method of claim 7, further comprising verifying whether one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval.